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... In fact CPU and clock **frequency** are two important ... Observation 3: In Ptolemy DE **domain**, the value of an ... The result shows that the **timing** refinement scheme can ...

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... hardware complexity • Complex and high **frequency** of interaction between ... in the function- time **domain**, ie it ... Data accesses Instruction **timing** Data-space state ...

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... nication and **frequency** of transactions between HW and SW. The **cosimulation** tool keeps two ... The designer can decide between **timing** accurate simulation ...

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D Desmet, M Esvelt, P Avasare, D Verkest, H De Man ... - Hardware/Software Codesign, 1999.(CODES'99) Proceedings of ..., 1999 - [ieeexplore.ieee.org](#)

... paper we propose a C++ based **cosimulation** and codesign ... including a rotor and **frequency domain** equalization, the ... have their own hardware **timing** controller (DSTU ...

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System-Level Performance Estimation Strategy for SW and HW - group of 5 »

A Allara, C Brandolese, W Fornaciari, F Salice, D ... - International Conference on Computer Design - doi.ieeeecs.org

... The timed **co- simulation** is based on software synthesis and ... of the theoretical model of hw and sw **timing** models will ... for the sw and hw **domains**, respectively. ...

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Timed Executable System Specification of an ADSL Modem using a C++ based Design Environment: A Case ...

DDMEP Avasare, SWD Verkest - imec.be

... Virtual Prototype ("seamless" **co-simulation**) Test system ... a rotor and **frequency domain** equalization, the ... their own hardware **timing** controller (DSTU ...

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AH Anderson, GA Shaw - The Journal of VLSI Signal Processing, 1997 - Springer

... common knowledge implicitly • span many **domains** of knowledge ... functionality, and data values and **timing** will be ... The maximum pulse repetition **frequency** of the ...

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16	BRS	L28	0	(mentor-graphic-corporation).as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWEN T; IBM_TDB	2006/09/22 15:10

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by a factor of 8/5, and at the **same time** produce a complex ... As is typical of **simulation domains**, the SDF domain does not have many targets. To ...

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combining multiple simulators or **simulation domains** sacrifices efficiency. ... systems, channels operate on **different frequencies** and are thus ...

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tems and **simulation domains**. 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 ... time-dependent as these Fourier components are observed at **different frequencies**. ...

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... to clock cycles or even phases within cycles in the **timing domain**. ... programming interface

(API) to interconnect the **instruction-set simulator** generated from the ...

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... and architectures in these application **domains** prohibits an ... eg, design size, power consumption, clock **frequency**) can be ... Fig.7. Specification of the **timing** model ...

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MJ Ammer, M Sheets, T Karalar, M Kuulusa, J Rabaey - DAC, June, 2003 - [doi.ieeeecomputersociety.org](#)

... the data and manage the gated clock **domains**. ... power by lowering the switching **frequency**

and allows ... power consumption while meeting the **timing** and flexibility ...

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P Schaumont, I Verbauwhede - Computer, 2003 - [ieeexplore.ieee.org](#)

... resist power and **timing** attacks. ... CPU Radio **frequency** ... Figure 7. The ThumbPod prototype

combines security, biometrics, and network- ing **domains**. ...

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 ... traces, ours also contain translation, **timing**, bus, and ... a particular segment of the public-**domain** ray-trace benchmark Table 3 presents the **frequencies** of the ...
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 ... C code is annotated with **timing** estimates predicting ... for programs from a different **domain**, the calibration ... in actual programs the relative **frequency** of one ...
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 ... the past work done in the **domain** of networks ... The **timing**, and area analysis for this implementation was ... **Instruction Set Simulator** (ISS) and the clock **frequency**. ...
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... modules (stars) in the Discrete Event domain of Ptolemy ... resources (such as CPU and clock frequencies), assign each ... to the event overflow, and timing consistency ...

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B Ramanadin, F Pogodalla - Rapid System Prototyping, 1996. Proceedings., Seventh IEEE ... , 1996 - [doi.ieeecomputersociety.org](#)

... The instruction set simulator allows generation of a ... Deep and meticulous timing analysis

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